What is claimed is:

1. A rate matching calculation method, comprising the steps of:

obtaining the number of increase or decrease bits on each channel for each frame, using data per frame on CCTrCH, the number of bits before rate matching in each TrCH to be transmitted on one frame simultaneously, and weight for each channel, according to the following equation (1);

obtaining a rate matching parameter on the basis of the number of increase or decrease bits on each channel for each frame,

wherein the number of increase or decrease bits on each channel for each frame is calculated by a corrected equation in which b/a is substituted for $b/a + 1/c^2$ in equation (1):

$$Z_{ij} = \left\lfloor \frac{\sum_{m=1}^{i} RM_m \cdot N_{mj}}{\sum_{m=1}^{I} RM_m \cdot N_{mj}} \cdot N_{dataj} \right\rfloor \quad for\ alli = 1..I \qquad (1)$$

(b: numerator sum; a: denominator sum; c: N_{dataj})

where RMi : rate matching attribute of TrCH#i

Ni,j : the number of bits per frame on TrCH#i

Ndata,j : the number of bits on CCTrCH

ΔNi,j : the number of increase or decrease bits on TrCH#i.

2. A rate matching calculation method, comprising the steps of:

obtaining the number of increase or decrease bits on each channel for each frame, using data per frame on CCTrCH, the number of bits before rate matching in each TrCH to be transmitted on one frame simultaneously, and weight for each channel, according to the following equation (1);

obtaining a rate matching parameter on the basis of the number of increase or decrease bits on each channel for each frame,

wherein in a case that a correct number of increase or decrease bits is not obtained by a combination of a, b and c, a predetermined the number of increase or decrease bits is output:

$$Z_{ij} = \left\lfloor \frac{\sum_{m=1}^{i} RM_{m} \cdot N_{mj}}{\sum_{m=1}^{I} RM_{m} \cdot N_{mj}} \cdot N_{data,j} \right\rfloor \quad for \ \ alli = 1..I \qquad (1)$$

(b: $\sum_{m=1}^{i} RM_{m} \cdot N_{mj}$; a: $\sum_{m=1}^{I} RM_{m} \cdot N_{mj}$; c: $N_{data,j}$)

where RMi : rate matching attribute of TrCH#i

Ni,j : the number of bits per frame on TrCH#i

Ndata,j : the number of bits on CCTrCH

ΔNi,j : the number of increase or decrease bits on TrCH#i.

3. A rate matching calculation method,

comprising the steps of:

obtaining the number of increase or decrease bits on each channel for each frame, using data per frame on CCTrCH, the number of bits before rate matching in each TrCH to be transmitted on one frame simultaneously, and weight for each channel, according to the following equation (1);

obtaining a rate matching parameter on the basis of the number of increase or decrease bits on each channel for each frame,

wherein the number of increase or decrease bits on each channel for each frame is obtained by calculating b×c and then dividing a result of the calculation by a:

$$Z_{ij} = \left\lfloor \frac{\sum_{m=1}^{j} RM_m \cdot N_{mj}}{\sum_{m=1}^{I} RM_m \cdot N_{mj}} \cdot N_{dataj} \right\rfloor \quad for \ alli = 1..I \qquad (1)$$

(b = numerator, a = denominator, c = N_{dataj})

where RMi : rate matching attribute of TrCH#i

Ni,j : the number of bits per frame on TrCH#i

Ndata,j : the number of bits on CCTrCH

ΔNi,j : the number of increase or decrease bits on TrCH#i.

4. The rate matching calculation method according to claim 3, wherein when the result of b×c exceeds 32 bits, the value of b×c is divided into upper

28 bits and lower 15 bits, a is subtracted from the upper 28 bits, "1" is set when the subtraction is enabled, while "0" is set when the subtraction is disabled, and after finishing the subtraction once, the upper 28 bits are shifted to the left by 1 bit, α is added to the lowest bit of the lower bits, and the subtraction of a and bit shift processing is performed repeatedly 17 times.

5. A rate matching apparatus comprising:

storage means for storing program data of an equation where $1/c^2$ is added to the result of b/a of the following equation (1) for use in obtaining the number of increase or decrease bits on each channel for each frame, using data per frame on CCTrCH, the number of bits before rate matching in each TrCH to be transmitted on one frame simultaneously, and weight for each channel:

$$Z_{ij} = \left\lfloor \frac{\sum_{m=1}^{i} RM_m \cdot N_{mj}}{\sum_{m=1}^{I} RM_m \cdot N_{mj}} \cdot N_{data,j} \right\rfloor \quad for\ all\ i = 1..I \qquad (1)$$

(b: $\sum_{m=1}^{i} RM_m \cdot N_{mj}$; a: $\sum_{m=1}^{I} RM_m \cdot N_{mj}$; c: $N_{data,j}$)

where RMi : rate matching attribute of TrCH#i

Ni,j : the number of bits per frame on TrCH#i

Ndata,j : the number of bits on CCTrCH

ΔNi,j : the number of increase or decrease bits on TrCH#i;

calculating means for calculating the number of

increase or decrease bits on each channel for each frame according to the program data stored in said storage means; and

rate matching calculating means for calculating a rate matching parameter on the basis of the number of increase or decrease bits on each channel for each frame obtained by said calculating means.

6. A rate matching apparatus comprising:

first storage means for storing program data of an equation where $1/c^2$ is added to the result of b/a of the following equation (1) for use in obtaining the number of increase or decrease bits on each channel for each frame, using data per frame on CCTrCH, the number of bits before rate matching in each TrCH to be transmitted on one frame simultaneously, and weight for each channel:

$$Z_{ij} = \left\lfloor \frac{\sum_{m=1}^{i} RM_m \cdot N_{mj}}{\sum_{m=1}^{I} RM_m \cdot N_{mj}} \cdot N_{dataj} \right\rfloor \quad for\ alli = 1..I \qquad (1)$$

(a = denominator, b = numerator, c = $\lfloor \cdot \rfloor$)

where RMi : rate matching attribute of TrCH#i

Ni,j : the number of bits per frame on TrCH#i

Ndata,j : the number of bits on CCTrCH

ΔNi,j : the number of increase or decrease bits on TrCH#i;

calculating means for calculating the number of

increase or decrease bits on each channel for each frame according to the program data stored in said first storage means;

second storage means for storing a combination of a, b and c where a result calculated by said calculating means is not a correct calculation result, and the correct calculation result in the combination;

outputting means for outputting combination stored in said second storage means substituting for the number of increase or decrease bits from said calculating means, in a case that a combination of a, b and c in inputting a, b and c is stored in said second storage means; and

rate matching calculating means for calculating a rate matching parameter on the basis of either of the number of increase or decrease bits on each channel from said calculating means or said outputting means.

7. A rate matching apparatus comprising:

storage means for storing program data of the following equation (1) for use in obtaining the number of increase or decrease bits on each channel for each frame, using data per frame on CCTrCH, the number of bits before rate matching in each TrCH to be transmitted on one frame simultaneously, and weight for each channel:

$$Z_{ij} = \left\lfloor \frac{\sum_{m=1}^{i} RM_m \cdot N_{mj}}{\sum_{m=1}^{I} RM_m \cdot N_{mj}} \cdot N_{dataj} \right\rfloor \quad for \ alli = 1..I \qquad (1)$$

(b, a, c)

where RMi : rate matching attribute of TrCH#i

Ni,j : the number of bits per frame on TrCH#i

Ndata,j : the number of bits on CCTrCH

ΔNi,j : the number of increase or decrease bits on TrCH#i; and

calculating means for in the equation indicated by the program data stored in said storage means, first calculating b×c, then dividing the result of b×c by a, and thereby obtaining the number of increase or decrease bits on each channel for each frame.

8. A rate matching apparatus according to claim 7, wherein in the case where the result of b×c exceeds 32 bits, said calculating means divides a value of b ×c into upper 28 bits and lower 15 bits, subtracts a from the upper 28 bits, sets "1" when the subtraction is enabled, while setting "0" when the subtraction is disabled, shifts the upper 28 bits to the left by 1 bit after finishing the subtraction once, adds a lowest bit of the lower bits to α, and repeatedly performs the subtraction of a and bit shift processing 17 times.

9. A base station apparatus comprising:

the rate matching apparatus according to any one of claims 5 to 8; and

a transmission/reception apparatus which inputs a frame extracted from a received signal to said rate matching apparatus at the time of receiving signals, while further inputting a frame to be transmitted to said rate matching apparatus at the time of transmitting signals.

10. A mobile station apparatus comprising:

the rate matching apparatus according to any one of claims 5 to 8; and

a transmission/reception apparatus which inputs a frame extracted from a received signal to said rate matching apparatus at the time of receiving signals, while further inputting a frame to be transmitted to said rate matching apparatus at the time of transmitting signals.